



CeraLink™ capacitor for fast-switching semiconductors

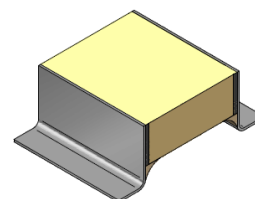
Low profile (LP) series

Series/Type:	0.5 μF, 700 V
Ordering code:	Z63000Z2910Z00 1Z15
Date:	2015-03-26
Version:	1.3

Preliminary data

Applications

- Designed for 900 V semiconductor modules
- Industrial power converters and inverters
- DC link / snubber capacitor for power converters and inverters



Features

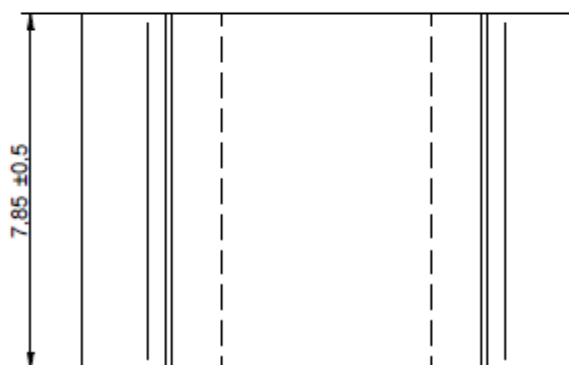
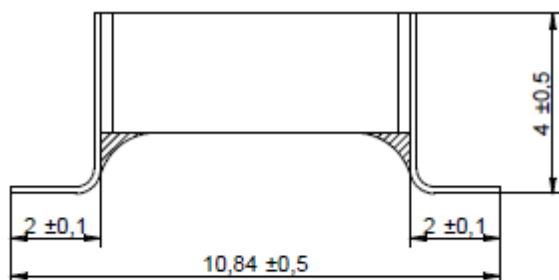
- High ripple current capability
- Low equivalent serial inductance (ESL)
- Low equivalent serial resistance (ESR)
- Low power loss
- Low dielectric absorption
- Optimized for high frequencies up to several MHz
- Increasing capacitance with DC bias up to operating voltage
- High capacitance density
- Minimized dielectric loss at high temperatures
- High reliability

Construction

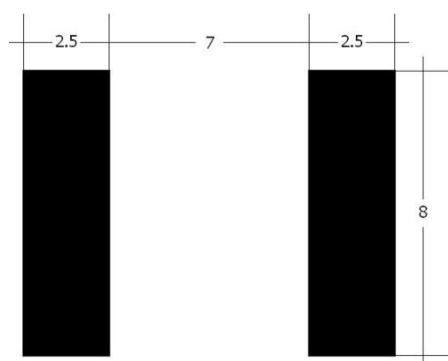
- RoHS-compatible PLZT ceramic (lead lanthanum zirconium titanate)
- Copper inner electrodes
- Silver outer electrodes
- Silver coated copper-invar lead frame
- Epoxy resin adhesive

Preliminary data

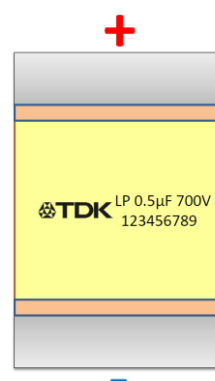
Dimensional drawings



Recommended solder pad:



Polarity:



Dimensions in mm

Preliminary data
Electrical specification

Operating voltage at maximum attenuation capability	V_{op}	= 600 V
Rated voltage	V_R	= 700 V
Withstand voltage (@ V _{ws} , 25 °C, 7 s)	V_{ws}	= 1000 V
Initial capacitance (@ 0 V _{DC} , 0.5 V _{RMS} , 1 kHz, 25 °C)	C₀	= 0.14 μF ± 20%
Typical effective capacitance (@ V _{op} , 0.5 V _{RMS} , 1 kHz, 25 °C)	C_{eff,typ}	= 0.26 μF
Typical nominal capacitance* (@ V _{op} , quasistatic, 25 °C)	C_{nom,typ}	> 0.5 μF
* See glossary (page 12) for definition of the nominal capacitance		
Dissipation factor (@ 0 V _{DC} , 0.5 V _{RMS} , 1 kHz, 25 °C)	tan δ	< 0.02
Insulation resistance (@ V _{op} , t > 240 s, 25 °C)	R_{ins,typ}	> 1 GΩ
Operating device temperature	T_{device}	- 40 °C... + 125 °C
Temperature range (limited time excursion 5% of operation time)	T_{device}	+ 125 °C... +150 °C
Weight of device		approx. 1.3 g

Typical values

ESR 0 V _{DC} , 0.5 V _{RMS} , 25 °C, 1 MHz	ESR 0 V _{DC} , 0.5 V _{RMS} , 25 °C, 1 kHz	ESL	I_{op}¹⁾ 100 kHz T _A = 85 °C	I_{op}¹⁾ 100 kHz T _A = 105 °C
mΩ	Ω	nH	A_{RMS}	A_{RMS}
18	13.7	2.5	5.4	4.4

¹⁾ Normal operation current without forced cooling at T_{device} = 125 °C. Higher values permissible at reduced life time.

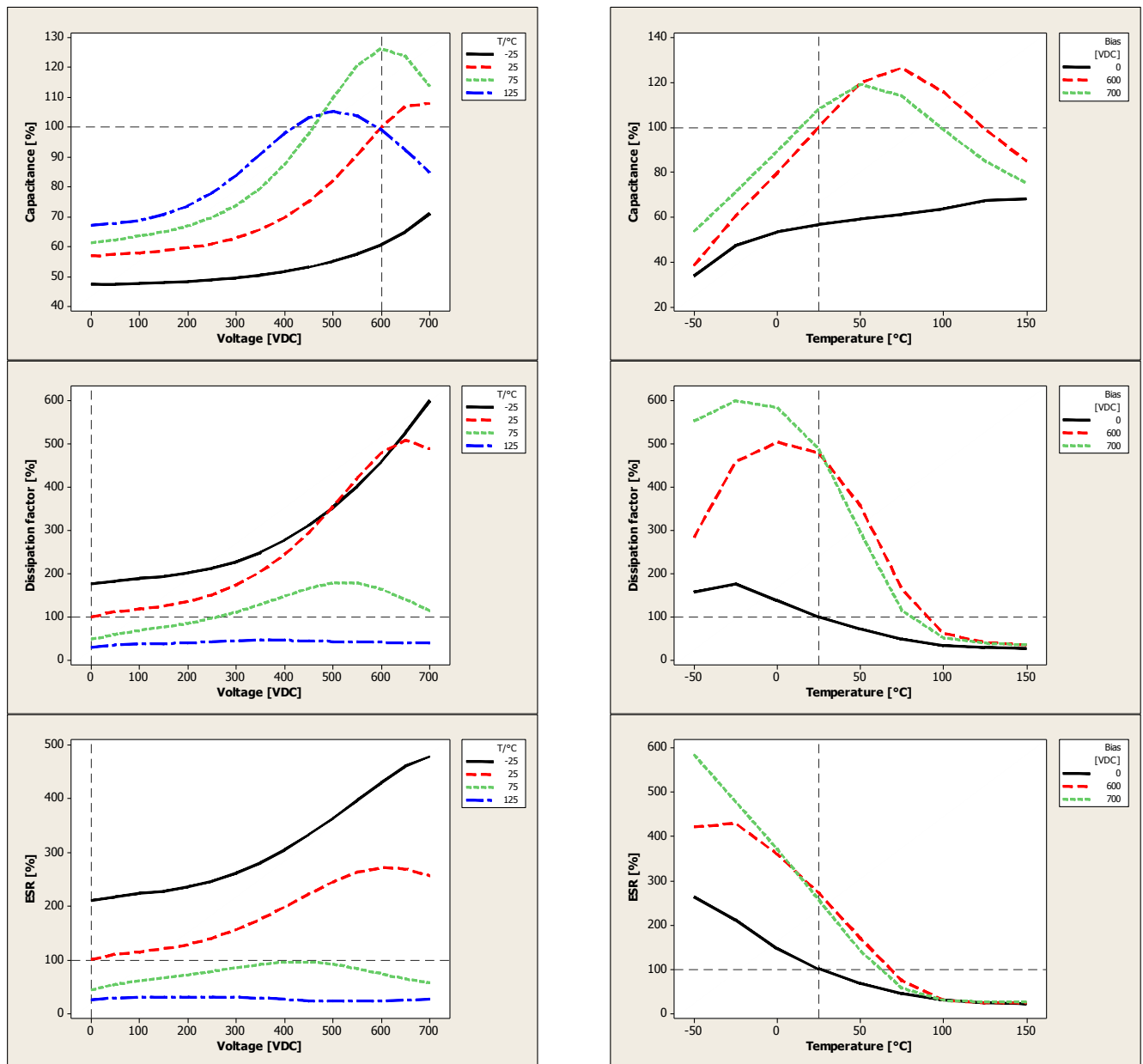
Preliminary data

Typical characteristics as a function of temperature and voltage

($V_{AC} = 0.5 V_{RMS}$, frequency = 1 kHz)

All given temperatures are device temperatures.

The curves show the relative changes of the capacitance, dissipation factor and ESR. The 100% values correspond to $C_{eff, typ}$ and $\tan \delta$ which are given on page 4 of this data sheet.



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Typical capacitance values as a function of voltage

Large signal capacitance:

Quasistatic (slow variation of the voltage), 25 °C

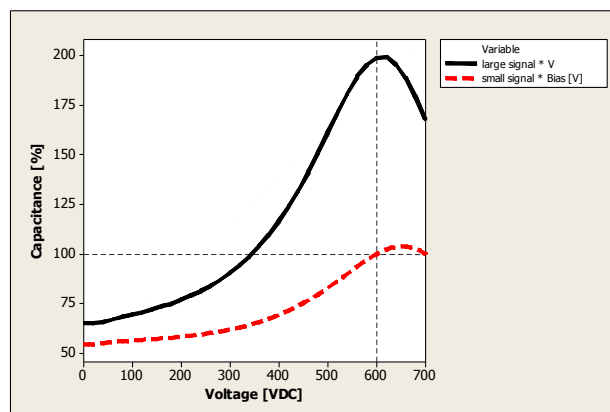
The nominal capacitance is defined as the large signal capacitance at V_{op} .

See glossary for further information.

Small signal capacitance:

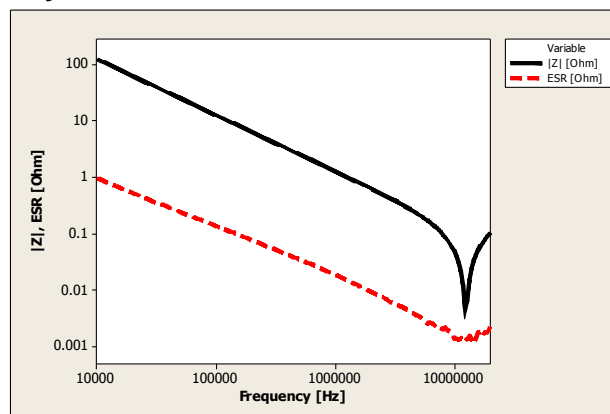
0.5 V_{RMS}, 1 kHz, 25 °C

The effective capacitance is defined as the small signal capacitance at V_{op} .



Typical impedance and ESR as a function of frequency

$V_{DC} = 0$ V, $V_{AC} = 0.5$ V_{RMS}, $T_{device} = 25$ °C

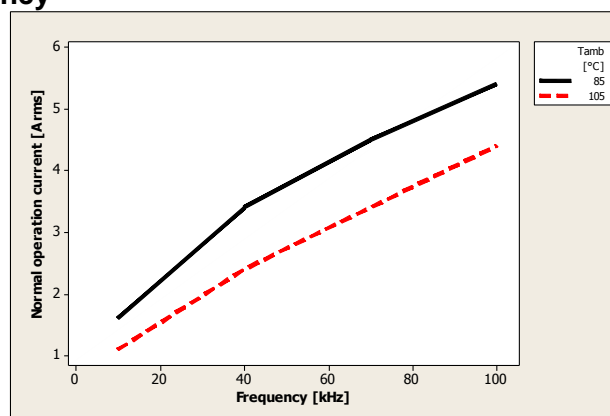


Typical permissible current as a function of frequency

Measurement performed at V_{op} .

The values correspond to a device temperature of 125 °C.

No active cooling was used.



Aging

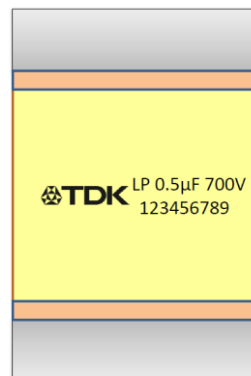
The capacitance has an aging behavior which shows a decrease of capacitance with time.

The typical aging rate is about 2.5% per logarithmic decade in hours.

Preliminary data

Marking of components

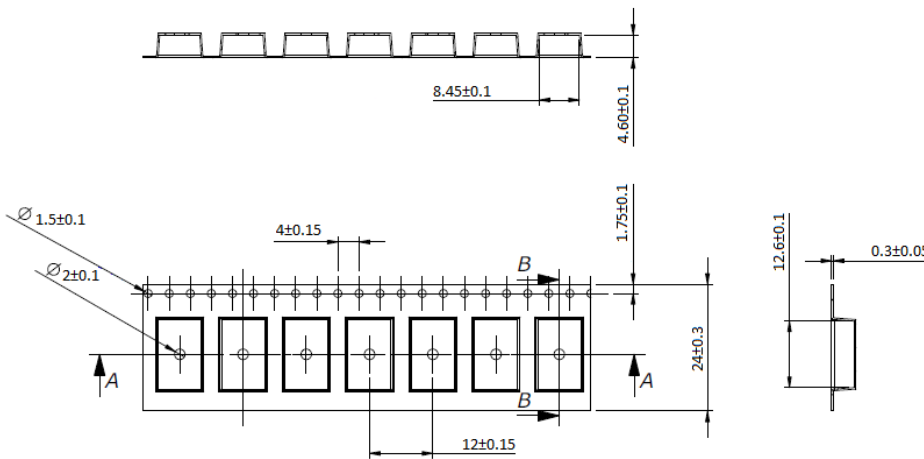
- Manufacturer's logo
- CeraLink™ type
- Nominal capacitance
- Rated voltage
- Lot number, 9 digits



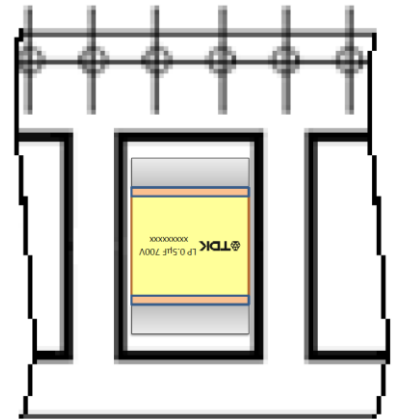
Preliminary data

Packaging

The CeraLink™ will be delivered in a blister tape and will be packed in a cardboard box.



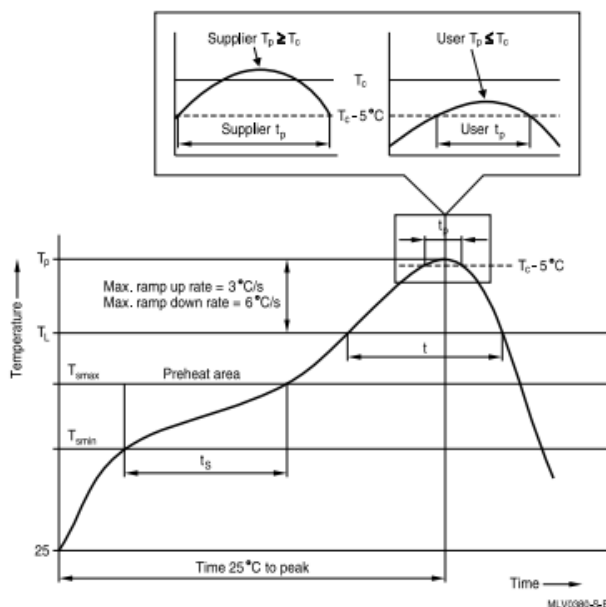
Part orientation:



Dimension in mm

Preliminary data

Recommended reflow soldering profile



Profile feature		SAC Sn95.5Ag3.8Cu0.7 N ₂ atmosphere
Preheat and soak		
- Temperature min	T_{smin}	150 °C
- Temperature max	T_{smax}	200 °C
- Time	t_{smin} to t_{smax}	60 ... 180 seconds
Average ramp-up rate	T_{smax} to T_p	3 °C/ second max.
Liquidus temperature	T_L	217 °C
Time at liquidus temperature	t_L	60 ... 150 seconds
Peak package body temperature	$T_p^{1)}$	245 °C ... 260 °C max. ²⁾
Time (t_p) ³⁾ within 5 °C of specified classification temperature (T_c)		30 seconds ³⁾
Average ramp-down rate	T_p to T_{smax}	6 °C/ second max.
Time 25 °C to peak temperature		maximum 8 minutes

1) Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

2) Depending on package thickness. For details please refer to JEDEC J-STD-020D.

3) Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

Notes:

All temperatures refer to topside of the package, measured on the package body surface.

Max. number of reflow cycles: 3

After the soldering process, the capacitance is lowered. Applying V_R to the device will re-establish the capacitance.

The components are suitable for reflow soldering to JEDEC J-STD-020D.

Preliminary data

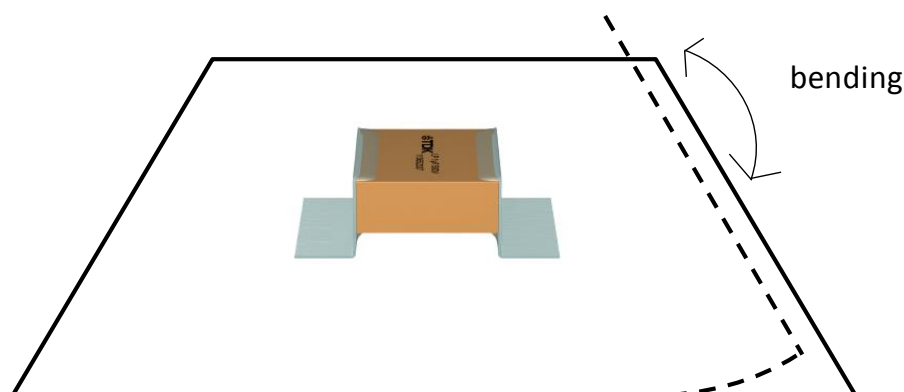
General technical information

Storage

- Only store CeraLink™ capacitors in their original packaging. Do not open the package prior to processing.
- Storage conditions in original packaging: temperature -25 °C to $+45\text{ °C}$, relative humidity $\leq 75\%$ annual average, maximum 95%, dew precipitation is inadmissible.
- Do not store CeraLink™ capacitors where they are exposed to heat or direct sunlight. Otherwise the packaging material may be deformed or CeraLink™ may stick together, causing problems during mounting.
- Avoid contamination of the CeraLink™ surface during storage, handling and processing.
- Avoid storing CeraLink™ devices in harmful environments where they are exposed to corrosive gases (e.g. SO_x, Cl).
- Use CeraLink™ as soon as possible after opening factory seals such as polyvinyl-sealed packages.
- Solder CeraLink™ components within 6 months after shipment from EPCOS.

Handling

- Do not drop CeraLink™ components or allow them to be chipped.
- Do not touch CeraLink™ with your bare hands - gloves are recommended.
- Avoid contamination of the CeraLink™ surface during handling.
- The CeraLink™ was tested to withstand the board flex test defined in the AEC-Q200 Rev. D, method 005.
- The CeraLink™ uses copper lead frames to prevent mechanical stress to the ceramic. Too much bending causes open mode. Avoid high mechanical stress like twisting after soldering on a PCB.

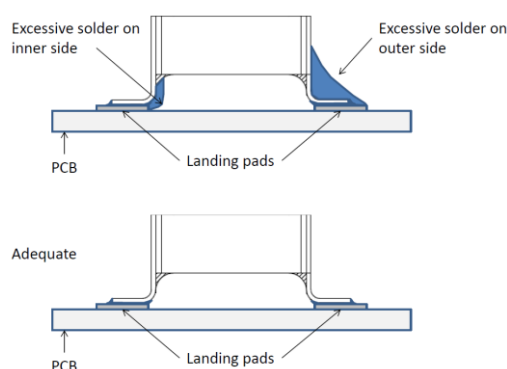


Preliminary data
Mounting

- Do not subject CeraLink™ devices to mechanical stress when encapsulating them with sealing material or overmolding with plastic material. Encapsulation may lead to worse heat dissipation too. Please ask for further information.
- Do not scratch the electrodes before, during or after the mounting process.
- Make sure contacts and housings used for assembly with CeraLink™ components are clean before mounting.
- The surface temperature of an operating CeraLink™ can be higher than the ambient temperature. Ensure that adjacent components are placed at a sufficient distance from a CeraLink™ to allow proper cooling.
- Avoid contamination of the CeraLink™ surface during processing.

Soldering guidelines

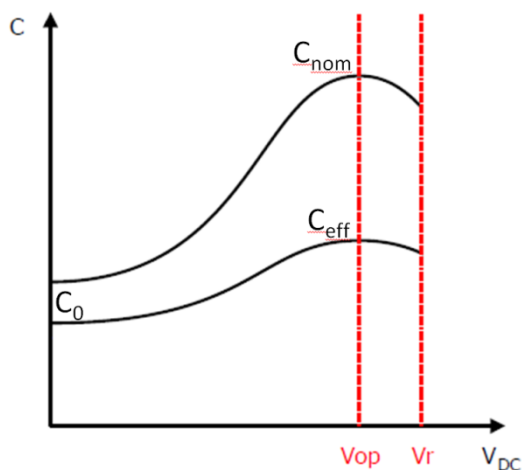
- The use of mild, non-activated fluxes for soldering is recommended, as well as proper cleaning of the PCB.
- Complete removal of flux is recommended to avoid surface contamination that can result in an instable and/or high leakage current.
- Use resin-type or non-activated flux.
- Bear in mind that insufficient preheating may cause ceramic cracks.
- Rapid cooling by dipping in solvent is not recommended, otherwise a component may crack.
- Excessive usage of solder paste can reduce the mechanical robustness of the device, whereas insufficient solder may cause the CeraLink™ to detach from the PCB. Use an adequate amount of solder paste, but on the landing pads only.



- If an unsuitable cleaning fluid is used, flux residue or foreign particles may stick to the CeraLink™ surface and deteriorate its insulation resistance. Insufficient or improper cleaning of the CeraLink™ may cause damage to the component.
- Excessive washing like ultrasonic cleaning, can affect the connection between the ceramic chip and the outer electrode. To avoid this, we give the following recommendation:
 - Power: 20 W/l max.
 - Frequency: 40 kHz max.
 - Washing time: 5 minutes max.

Preliminary data

Glossary



Initial capacitance C_0 :

is the value at the origin of the hysteresis without any applied direct voltage.

Effective capacitance C_{eff} :

occurs at V_{op} and is measured with an applied ripple voltage of $0.5 V_{RMS}$ and 1 kHz. The CeraLink™ is designed to have its highest capacitance value at the operating voltage V_{op} .

Nominal capacitance C_{nom} :

is the value derived by the tangent of the mean hysteresis as the derivation of the mean hysteresis is $dQ/dV \sim C$.

Preliminary data
Symbols and terms

AC	Alternating current
C_0	Initial capacitance
$C_{\text{eff,typ}}$	Typical effective capacitance
$C_{\text{nom,typ}}$	Typical nominal capacitance
DC	Direct current
ESL	Equivalent serial inductance
ESR	Equivalent serial resistance
I_{op}	Operation ripple current, root mean square value of sinusoidal AC current
LP	Low profile
PCB	Printed circuit board
PLZT	Lead lanthanum zirconium titanate
R_{ins}	Insulation resistance
SAC	Tin silver copper alloy; lead-free solder paste
T_A	Ambient temperature
$\tan \delta$	Dissipation factor
T_{device}	Device temperature. $T_{\text{device}} = T_A + \Delta T$ (ΔT defines the self-heating of the device due to applied current).
V_{op}	Operation voltage
V_R	Rated voltage
V_{RMS}	Root mean square value of sinusoidal AC voltage
V_{ws}	Withstand voltage
ΔT	Increase of temperature during operation

Preliminary data

Cautions and warnings

General

Not for use in resonant circuits, where a voltage of alternating polarity occurs.

Not for AC applications. Consult your EPCOS representative for further details.

If used in snubber circuits, ensure that the sum of all voltages remains at the same polarity.

Some parts of this publication contain statements about the suitability of our CeraLink™ components for certain areas of application, including recommendations about incorporation/design-in of these products into customer applications. The statements are based on our knowledge of typical requirements often made of our CeraLink™ devices in the particular areas. We nevertheless expressly point out that such statements cannot be regarded as binding statements about the suitability of our CeraLink™ components for a particular customer application. As a rule, EPCOS is either unfamiliar with individual customer applications or less familiar with them than the customers themselves. For these reasons, it is always incumbent on the customer to check and decide whether the CeraLink™ devices with the properties described in the product specification are suitable for use in a particular customer application.

- Do not use EPCOS CeraLink™ components for purposes not identified in our specifications.
- Ensure the suitability of a CeraLink™ in particular by testing it for reliability during design-in. Always evaluate a CeraLink™ component under worst-case conditions.
- Pay special attention to the reliability of CeraLink™ devices intended for use in safety-critical applications (e.g. medical equipment, automotive, spacecraft, nuclear power plant).

Design notes

- Consider derating at higher operating temperatures. As a rule, lower temperatures and voltages increase the life time of CeraLink™ devices.
- If steep surge current edges are to be expected, make sure your design is as low-inductive as possible.
- In some cases the malfunctioning of passive electronic components or failure before the end of their service life cannot be completely ruled out in the current state of the art, even if they are operated as specified. In applications requiring a very high level of operational safety and especially when the malfunction or failure of a passive electronic component could endanger human life or health (e.g. in accident prevention, life-saving systems, or automotive battery line applications such as clamp 30), ensure by suitable design of the application or other measures (e.g. installation of protective circuitry, fuse or redundancy) that no injury or damage is sustained by third parties in the event of such a malfunction or failure.
- Specified values only apply to CeraLink™ components that have not been subject to prior electrical, mechanical or thermal damage. The use of CeraLink™ devices in line-to-ground applications is therefore not advisable, and it is only allowed together with safety countermeasures such as thermal fuses.

Preliminary data

Operation

- Use CeraLink™ only within the specified operating temperature range.
- Use CeraLink™ only within specified voltage and current ranges.
- The CeraLink has to be operated in a dry atmosphere, which must not contain any additional chemical vapors or substances.
- Environmental conditions must not harm the CeraLink™. Use the capacitors under normal atmospheric conditions only. A reduction of the oxygen partial pressure to below 1 mbar is not permissible.
- Prevent a CeraLink™ from contacting liquids and solvents.
- Avoid dewing and condensation.
- During operation, the CeraLink™ can produce audible noise due to its piezoelectric characteristic.
- EPCOS CeraLink™ components are mainly designed for encased applications. Under all circumstances avoid exposure to:
 - direct sunlight
 - rain or condensation
 - steam, saline spray
 - corrosive gases
 - atmosphere with reduced oxygen content

This listing does not claim to be complete, but merely reflects the experience of EPCOS AG.

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